ESD-TR-91-085

Technical Report
925

Shallow-Buried-Channel CCDs with Built-In Drift Fields

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12 July 1991

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Prepared for the Department of the Air Force
under Contract F19628-90-C-0002.

This report is based on studies performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology. The work was sponsored by the Department of the Air Force under Contract F19628-90-C-0002.

The ESD Public Affairs Office has reviewed this report, and it is releasable to the National Technical Information Service, where it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

Hugh L. Southall

Hugh L. Southall, Lt. Col., USAF
Chief, ESD Lincoln Laboratory Project Office

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

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Group 86

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ACKNOWLEDGMENTS

The authors thank the Lincoln Laboratory Innovative Research Program committee for its support and encouragement; Duane R. Arsenault, Mark M. Seaver, and David B.Whitley for their assistance in the design and testing of the CCDs; and John Melngailis, Jim E. Murguia, and Mark I. Shepard of MIT for suggesting and carrying out the focused ion beam implantation. We further thank Dick Bredthauer at Ford Aerospace for the successful fabrication of the CCDs.

This work was sponsored by the Department of the Air Force.

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1. INTRODUCTION

In charge-coupled devices (CCDs) the charge representing the information to be processed is stored in potential wells formed under gate electrodes and transferred from well to well. The storage and transfer of the charge are directly controlled by the voltage applied to the gates and are strongly influenced by the structure parameters, such as channel doping profile and electrode geometry.

Charge-transfer efficiency (CTE) is one of the most important measures of CCD performance. Current technology has improved to the point that CCDs can have, at low speed, a CTE better than 0.99999 per transfer. At high speeds, however, the CTE can be severely degraded if not enough time is allowed for electrons to travel to the next stage. There are three basic charge-transfer mechanisms: self-induced drift (Coulomb repulsion), thermal diffusion, and drift due to fringing fields [1]. Initially, the bulk of the charge packet transfers to the next potential well very rapidly by Coulomb repulsion, but below a certain charge density the self-repulsion becomes negligible and, in the absence of drift fields, thermal diffusion dominates the transfer. Diffusion is a relatively slow process and therefore limits the speed at which the devices can be operated.

The CCD speed can be enhanced by designing structures with strong fringing fields in the channel, such as deep-buried-channel CCDs. Deep-buried-channel delay lines have indeed been demonstrated at hundreds of megahertz [1], but they have several disadvantages that may ultimately limit their usefulness. For example, the shape of the potential wells is distorted, degrading linearity and affecting the overall signal-processing performance of the CCD. Furthermore, the charge-handling capacity decreases as the channel moves into the bulk, and clocks of at least 10 V are required to maintain sufficient charge capacity in the wells. These 10-V clocks are not only difficult to generate at high speed but are incompatible with the 5-V technology necessary for the high-performance on-chip support circuits that interface with the CCD.

The goal of this Innovative Research Program (IRP) project was to design and build shallow-buried-channel CCDs that would run at high speed with 5-V clocks. Although the charge transfer in these CCDs is not affected by surface states and the charge mobility is that of the bulk Si, the well characteristics are similar to surface-channel CCDs. The large charge capacity and linearity come at the expense of fringing fields. Developing CCDs with a built-in potential gradient to enhance the drift and improve the CTE would theoretically compensate for the lack of strong coupling between the gates.

The test structures were short-channel CCDs with storage gates 7 μm long and long-channel CCDs with storage gates 26 μm long. In both cases the barrier electrodes were 4 μm long. In general, short-channel CCDs ($L < 10$ μm) are used in signal-processing applications where speed is of maximum importance. Long-channel CCDs ($L > 10$ μm) are needed in applications that require the greater resolution, dynamic range, and noise immunity obtainable with the larger charge capacity or in imagers where pixel dimensions determine the CCD geometry.

An analog memory chip was also designed and fabricated with the linear CCDs. The chip has a serial-parallel-serial (SPS) architecture [2] and consists of a high-speed input register, a parallel array, and a low-speed output register.

The project was extremely successful. A dramatic effect of the built-in fields was demonstrated. Long-channel CCDs with built-in drift fields are more than an order of magnitude faster than the uniform CCDs (Figure 1). In addition, the electric field overcomes imperfections and reduces bulk trapping in the channel, resulting in improved performance even at very low speeds. Short-channel CCDs with the built-in drift fields were tested up to 370 MHz (the limit of the existing clock drivers) with no measurable degradation in the CTE, while the equivalent uniform CCDs degrade at 240 MHz (Figure 1). These results are consistent with two-dimensional computer simulations that consider only the transfer time of a single electron traveling down the calculated channel potential.

In this report the different structures tested and the details of the fabrication steps that generated the built-in fields will be described. The modeling and design of the CCDs, the experimental setup for the high-speed testing, and the experimental results will be discussed. Finally, the implications of these results on future programs will be addressed.

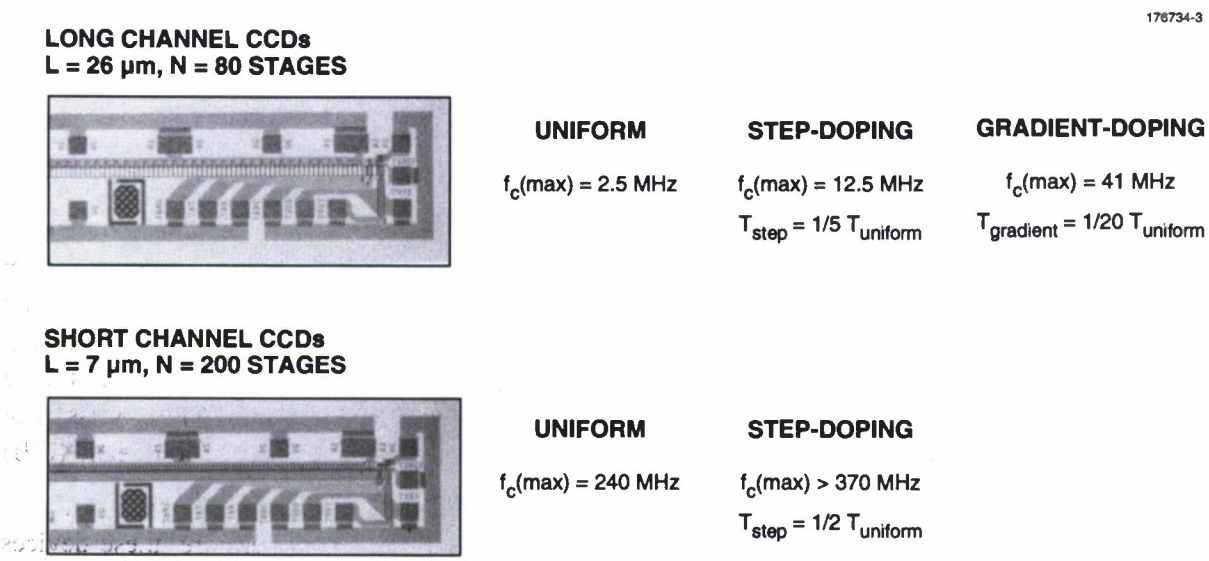

Figure 1. Pictures of the long- and short-channel CCDs and the measured maximum clocking rate $f_{c(max)}$ for the uniform and nonuniform cases. $T_{uniform}$, T_{step}, and $T_{gradient}$ are the corresponding transit times.

2. SHALLOW-BURIED-CHANNEL CCDs WITH BUILT-IN FIELDS

Long- and short-channel CCDs with storage gates 26 and 7 μm long, respectively, and more complex two-dimensional SPS memories have been studied. Each CCD with built-in fields was compared with a corresponding CCD fabricated with uniformly doped storage wells. For simplicity they are referred to here as nonuniform and uniform, respectively.

The CCDs and the fabrication process were based on an SPS memory chip recently designed at Lincoln Laboratory. The CCDs were fabricated at Ford Aerospace with an NMOS process, which included a 4-μm minimum feature size and three levels of polysilicon. The n-channel CCDs had a channel depth of 300 nm, a barrier electrode length of 4 μm, and a storage electrode length of 26 or 7 μm. After an initial uniform phosphorus implant to define the buried channel, the barrier electrodes (first polysilicon) were defined, and a second phosphorus implant was added to create the storage wells [Figure 2(a)]. Given the time and budget constraints of the IRP project, the basic process for which the implant parameters had been established in the past was left intact, even if the barrier-storage potential difference was smaller than the 2.5 V that would maximize the drift fields of the uniform CCDs. Increasing the barrier-storage potential difference would also increase the charge capacity that is currently calculated at 1500 $e/\mu m^2$.

The built-in fields were obtained by adding an additional implant to the storage wells. A nonuniform profile was obtained by adding a third phosphorus implant in the second half of each storage well [Figure 2(b)]. Preliminary simulations suggested that in the short-channel CCDs the built-in drift fields generated by the single step combined with the coupling fields would result in large drift fields everywhere along the storage wells during transfer. In the long-channel CCDs, however, the step was 13 μm from the edge of the wells. The drift fields in these 13-μm regions would be enhanced by the step doping but would be still relatively small. Making gradient-doped CCDs by implanting a gradient instead of a single step [Figure 2(c)] was proposed in order to distribute the built-in drift fields more evenly along the storage gates. The step doping was realized by adding an extra mask level to the standard CCD process. The gradient doping was obtained by direct writing the desired profile using the focused-ion-beam (FIB) technology available at MIT [3,4].

Ford Aerospace had reliably made similar uniform CCDs in the past. Furthermore, these devices were small, the design did not stress the technology, and the design was quite tolerant of fabrication imperfections. Even if there were delays due to processing, the basic fabrication was not considered to be a major risk factor. The riskiest aspect of the project was the gradient implant. The first fabrication steps were performed as usual at Ford Aerospace. After the storage implant, three wafers were shipped to MIT for the FIB implant. The others received the step implant and were then completed. After the FIB implant, the three wafers were sent back to Ford Aerospace where they were completed.

Given the limited resources of the IRP project, testing the calibration of the FIB machine and studying its performance with the special requirements of CCD channel implantation was not possible. In fact, one of the machine's most sophisticated features, the small ion beam and the resulting high spatial resolution (necessary to fabricate ultrasmall devices), turned out to be a significant problem. The beam was defocused as much as possible (about 1 μm) to dilute the dose and then overlapped the implant paths

to get acceptable uniformity. The machine is not normally used to implant devices that are as large as the CCDs. The total implant time was about 5 min per CCD and several hours per wafer. Sometimes during these long runs, the parameters of the beam (position or dose) drifted and the implant had to be interrupted.

While the yield was poor, the ultimate success of the FIB experiment was due to the MIT team that showed great ingenuity and determination, even when it was discovered that the alignment marks for the FIB had been destroyed because of an error in the masks or when it seemed that the Lincoln Laboratory computer-aided-design tools and the MIT chip-layout software were hopelessly incompatible.

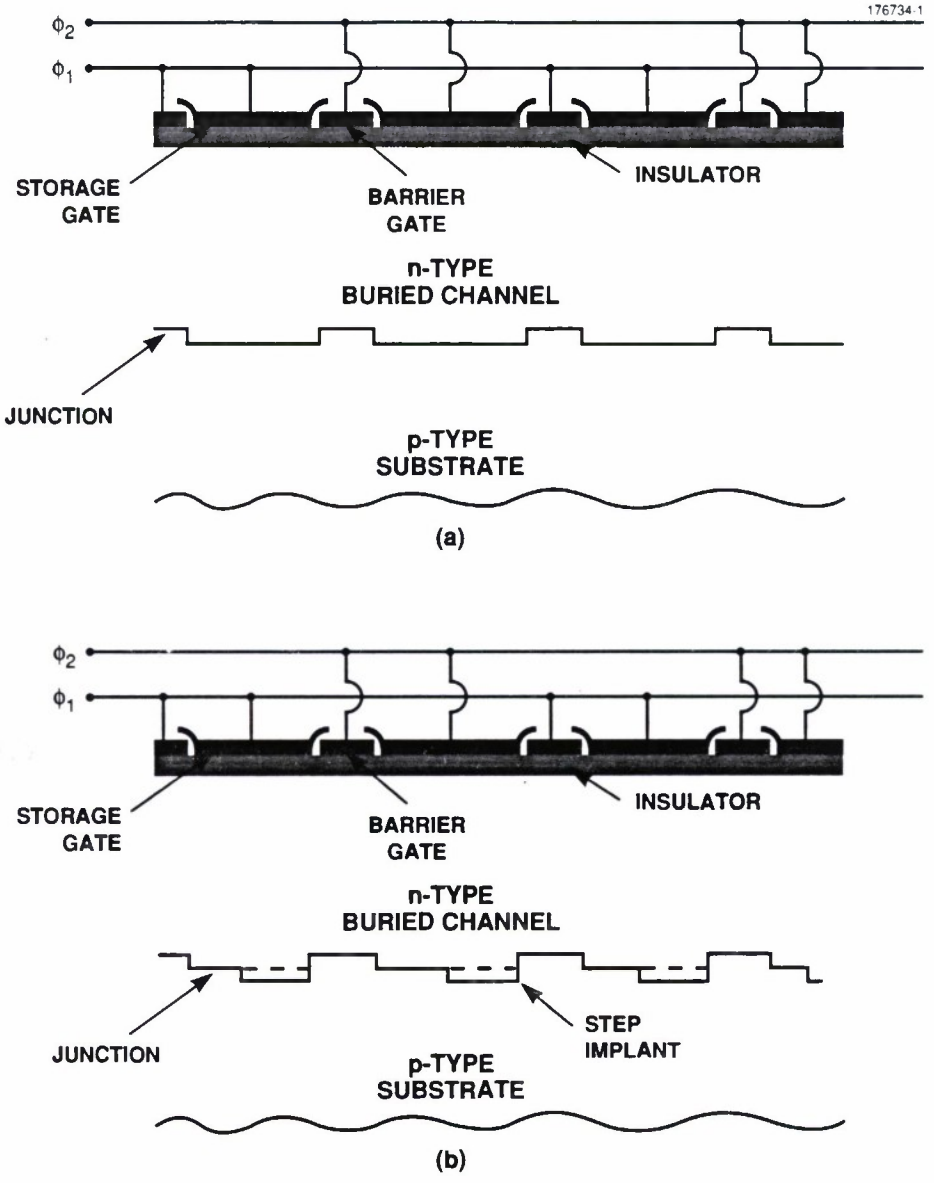

Figure 2. Two-phase buried-channel CCD structures: (a) uniform CCD and (b) step-doped CCD.

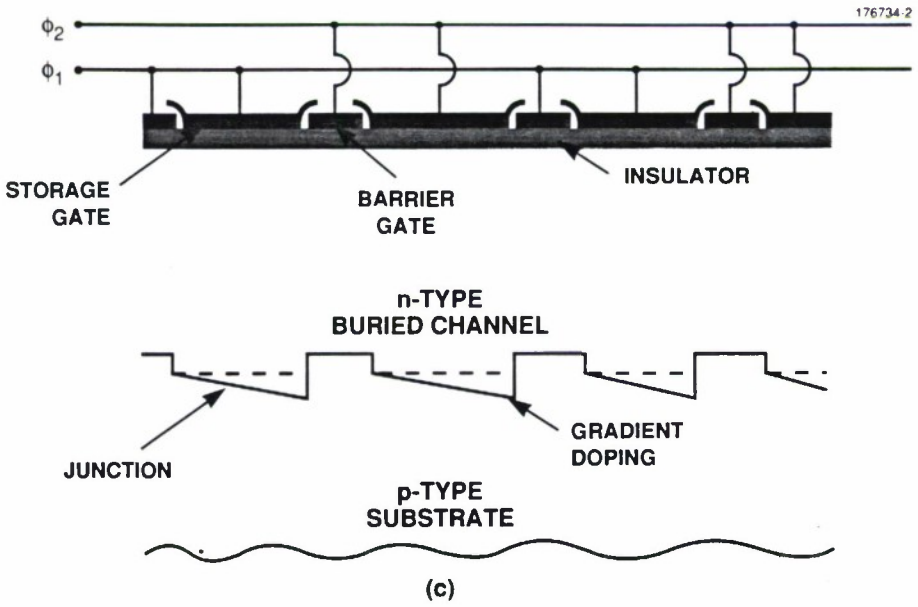

Figure 2 (continued). Two-phase buried-channel CCD structures: (c) gradient-doped CCD.

3. CCD MODELING

Although neither the alignment nor the exact dose is critical to enhance the drift fields, the nonuniform CCDs had to be designed with care to ensure that the extra implants were a small perturbation. In particular the process had to ensure that extra doping did not make the wells so deep that they did not clear the following barrier, preventing complete transfer at any clocking rate. The charge capacity is clearly increased in the nonuniform CCDs. However, because these CCDs are usually operated with a fat zero, neither the signal dynamic range nor the linearity is affected.

Without attempting to optimize the step doping, the uniformly doped and step-doped CCDs were modeled with CANDE, a two-dimensional device simulator. To estimate the effect of a small potential step ($\Delta V \approx 0.5$ V), the channel potential and electric field for empty wells was derived (the last few electrons did not affect the channel potential significantly). Figure 3(a) shows the predicted channel potential for the uniformly doped long-channel CCDs. Away from the edges the potential of the uniform CCDs is very flat and the electric field small (a few volts/cm). Figure 3(b) shows the calculated channel potential of the step-doped CCDs for a step $\Delta V \approx 0.5$ V. The electric field in this case is always more than 30 V/cm and grows very rapidly toward the center of the storage gates (where the step doping begins). Figure 3(c) shows the calculated channel potential of the gradient-doped CCDs. The gradient was approximated by five equal steps that added to a total perturbation of $\Delta V \approx 0.5$ V. In this case the potential is gently sloping and corresponds to a relatively large electric field everywhere in the channel. The electric field in this case is always more than 250 V/cm. From the channel electric field the single-electron transit time [1] was calculated to be 150, 20, and 6 ns for the uniform, step-doped, and gradient-doped CCDs, respectively. The predicted channel potential for the uniform and step-doped short-channel devices is shown in Figures 4(a) and (b). The corresponding single-electron transit times are, respectively, 0.8 and 0.4 ns.

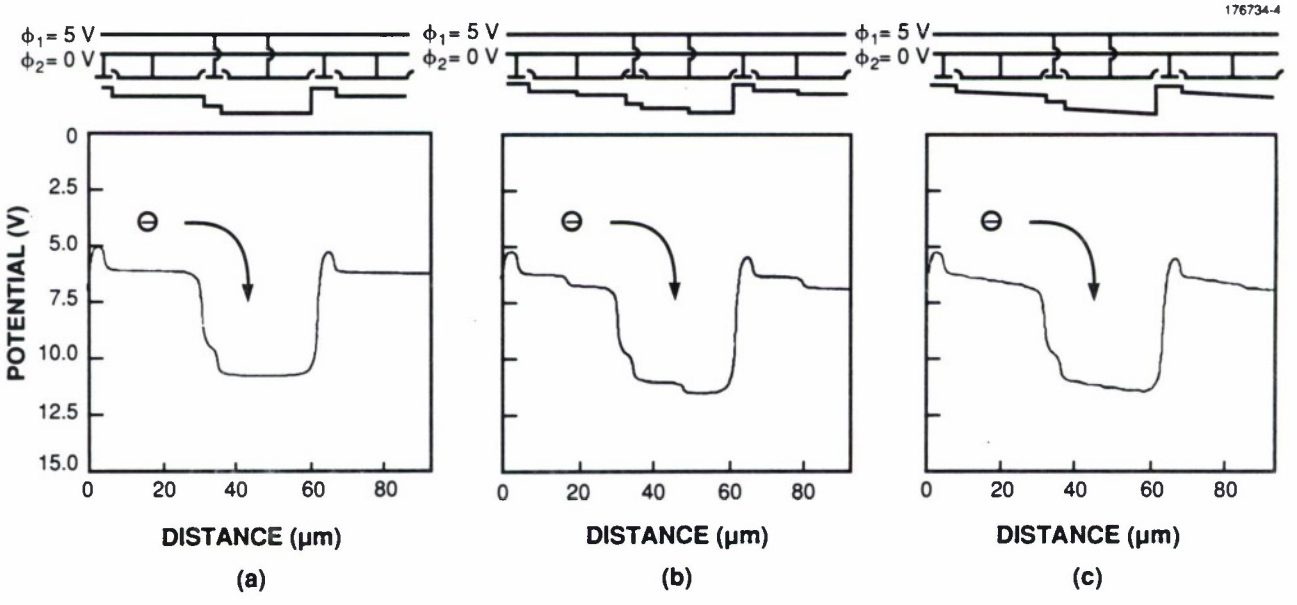

Figure 3. Channel potential calculated with CANDE for (a) uniformly doped, (b) step-doped, and (c) gradient-doped CCDs with 4-μm barrier gates and 26-μm storage gates.

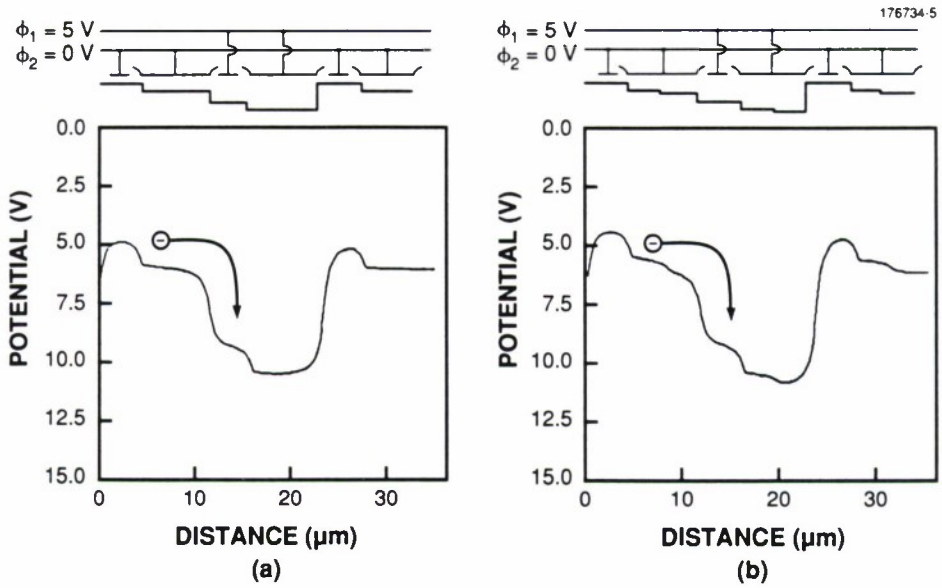

Figure 4. Channel potential calculated with CANDE for (a) uniformly doped and (b) step-doped CCDs with 4-μm barrier gates and 7-μm storage gates.

From the simple calculation of the single-electron drift, which ignores diffusion, the improvement in the CTE or the maximum clocking rate cannot be predicted. The calculations, nevertheless, indicate that even a small potential step can result in a significant enhancement in the electron drift.

4. EXPERIMENTS

4.1 EXPERIMENTAL SETUP

The devices tested are simple delay lines, designed so that the input, transfer, and output clocking speed can be independently set. The CTE was measured in slow-in, fast-transfer, slow-out experiments. The experimental setup is shown in Figure 5. The low-speed waveforms are generated by a programmable pattern generator (maximum speed: 125 MHz). The high-speed transfer clocks are generated by a high-speed, variable-frequency but nonprogrammable pulse generator. The select input of a high-speed multiplexer determines the number of high- and low-speed transfers in the CCD. The biggest challenge in the test setup was the high-speed (5 V) clock drivers.

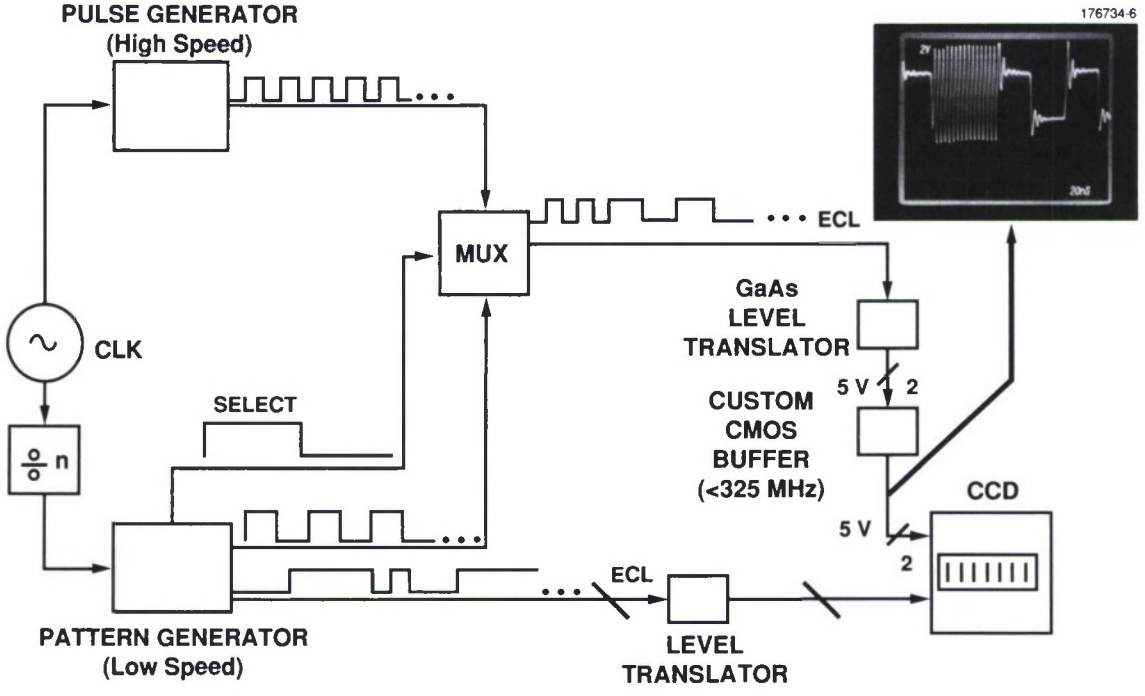

Figure 5. Test setup schematic. A master clock synchronizes the pulse generator (triggered at a frequency f_c) and the pattern generator (triggered at a frequency f_c/n). A select signal determines the number of high- and low-speed transfers through a multiplexer. Low-speed waveforms are converted to 5 V with conventional level shifters, while the high-speed transfer clocks are converted to 5-V signals capable of driving the CCD by a GaAs level translator and a custom CMOS buffer.

The clock drivers consist of a GaAs level translator, which converts emitter-coupled-logic (ECL) waveforms to 5 V, and a monolithic CMOS buffer that was designed at Lincoln Laboratory. These components were, at first, mounted on a two-sided board. The high-speed clocks were then fed into the CCDs (which were on a different board). The connections were kept as short as possible. With this setup

the CCDs could be tested up to 325 MHz. Above that frequency the GaAs level translator started oscillating and the clocks were lost. The problems with this relatively simple test board had been anticipated; therefore, a budget for improved clock drivers was incorporated in the project. In the new clock drivers all components (including the CCDs) were mounted on a multilayer board that provided better shielding and reduced parasitic capacitance and inductance.

The uniform and nonuniform CCDs are identical except for the extra implant to enhance the drift fields. The CCDs were tested by applying at low speed a single square pulse, five sample clocks long, corresponding to full amplitude. No fat zero was used. The signal was then transferred the length of the shift register at high speed. The output was read out at low speed. The CTE was generally constant up to a maximum clocking rate $f_{c(max)}$, beyond which it degraded very rapidly. From $f_{c(max)}$ the time T_t required for almost all the electrons to transfer can be estimated. For clock edges t_r and t_f,

$$f_{c(max)} = \frac{1}{2T_t + t_r t_f} \tag{1}$$

or

$$T_t = \frac{1}{2}\left(\frac{1}{f_{c(\max)}} - t_r - t_f\right). \tag{2}$$

For these experimental conditions, $t_r \approx t_f \approx 0.8$ to 1 ns.

4.2 LONG-CHANNEL CCDs

The experimentally determined $f_{c(max)}$ for the uniform, step-doped, and gradient-doped long-channel CCDs are 2.5, 12.5, and 41 MHz, respectively. From $f_{c(max)}$ the corresponding time T_t required for almost all the electrons to transfer can be estimated: $T_{t(uniform)} = 200$ ns, $T_{t(step)} = 40$ ns, and $T_{t(gradient)} = 10$ ns. The output signal for transfer at 2.5, 12.5, and 41 MHz is shown in Figure 6. In addition to the improvement in maximum clocking rate, the built-in fields improve the CTE even at low clocking rates. In the uniform CCDs the drift fields are so low that any imperfections can result in small potential troughs or bumps in the channel that can puddle charge and degrade the CTE. The built-in fields can wash out these imperfections and improve the CTE even at low clocking rates. Similarly, even if the maximum clocking rate is higher, the CTE of the gradient-doped CCDs is poorer than that of the step-doped CCDs. This result is probably caused by the finite width of the ion beam used for the direct-write implant or by small variations in its current during the implant, which result in an uneven channel potential. More experiments are needed to determine the exact cause of this roughness, which can probably be eliminated by further defocusing the width of the FIB.

The previous experiments were carried out at room temperature. For long-wavelength imaging applications, the CCDs have to be cooled to cryogenic temperatures where bulk trapping has been shown to degrade the CTE [5]. To determine if the built-in drift fields could improve the performance of infrared imagers, the CCDs were tested at 77 K. The experimental results are encouraging (Figure 7). Although the overall performance is degraded by the bulk trapping, the charge loss in the nonuniform CCDs is smaller than the charge loss in the uniform CCDs. The mechanism for this improvement can be understood by considering that when drift fields are strong enough (i.e., in the nonuniform CCDs) any charge emitted by the traps can rapidly drift and join its corresponding charge packet [5].

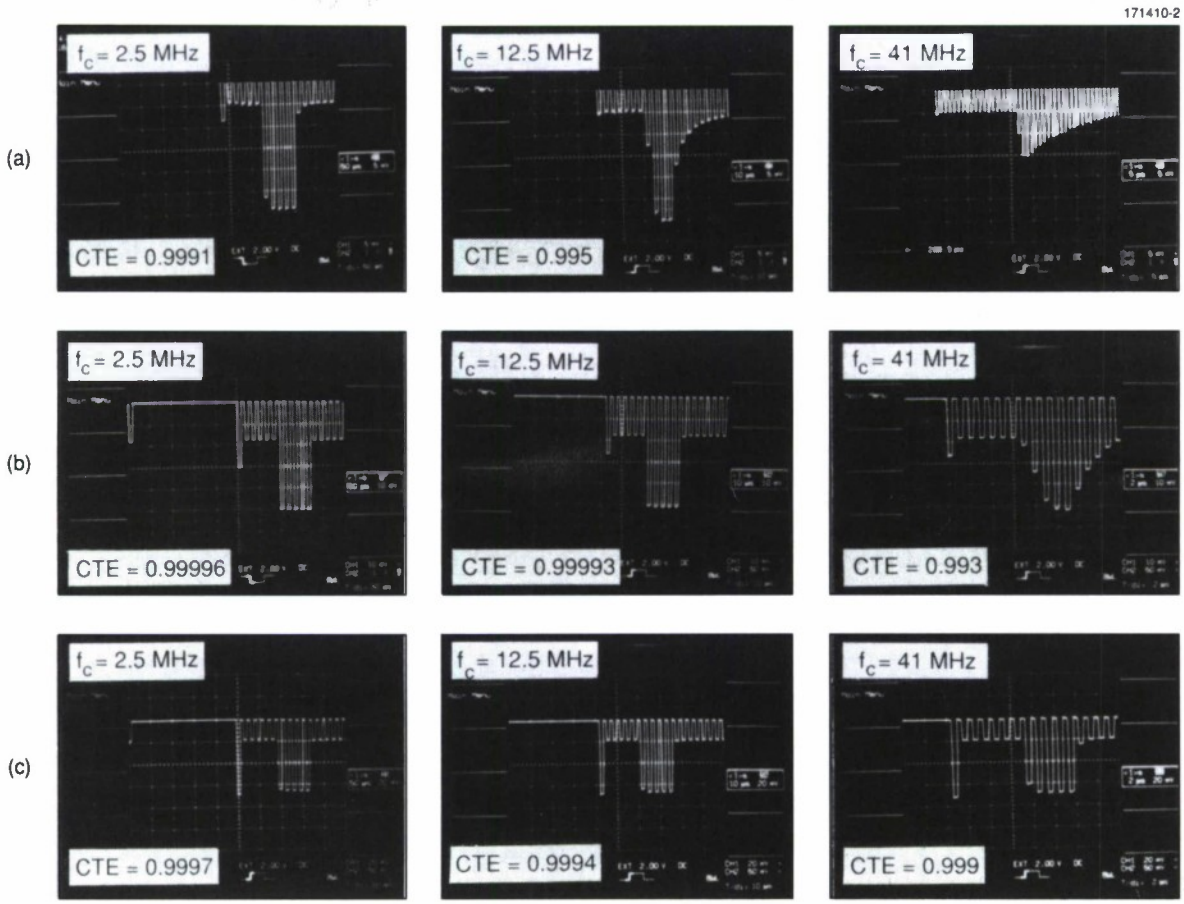

Figure 6. Output from (a) uniformly doped, (b) step-doped, and (c) gradient-doped long-channel CCDs at room temperature when the input is one pulse, five clock periods long, for the following cases: f_c = 2.5 MHz, f_c = 12.5 MHz, and f_c = 41 MHz.

4.3 SHORT-CHANNEL CCDs

The output signals for transfer at 240 and 325 MHz for both the uniformly doped and step-doped CCDs are shown in Figure 8. The transfer loss in the uniformly doped CCDs is too small to measure for f_c < 240 MHz (CTE > 0.99996) but increases very rapidly for higher clocking rates. The response of the corresponding CCDs with the built-in drift fields shows that even at 325 MHz, the transfer loss is barely measurable (CTE = 0.99995). As explained before, 325 MHz was the limit of the initial clock drivers. With the multilayer board the short-channel CCDs could be tested up to 370 MHz. The nonuniform CCD response for $f_{c(max)}$ = 370 MHz is shown in Figure 9. Unfortunately, the digital scope with which the CTE was previously measured was not available to test the CCDs at 370 MHz. With the available scope the CTE could not be measured. However, there was no observable difference between the output for a high and a low clocking rate, which indicates that $f_{c(max)}$ > 370 MHz for the step-doped, short-channel CCDs.

The transfer time corresponding to $f_{c(max)}$ = 240 MHz is 1.1 ns. Given the limitations of the existing clock drivers, one can only conclude that for the step-doped CCDs the transfer time is less than 0.5 ns.

The experimentally measured improvement in the transfer time for the long- and short-channel CCDs is consistent with the expectations and indicates that built-in drift fields can significantly improve the performance of CCDs at high speed.

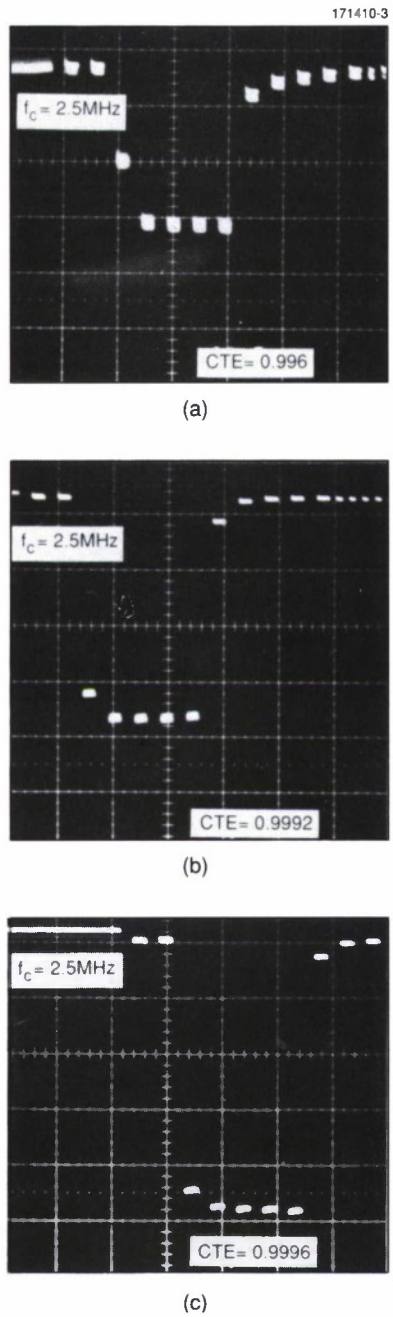

Figure 7. Output from (a) uniformly doped, (b) step-doped, and (c) gradient-doped long-channel CCDs when the input is one pulse, five clock periods long, the clocking rate is f_c = 2.5 MHz, and the temperature is 77 K.

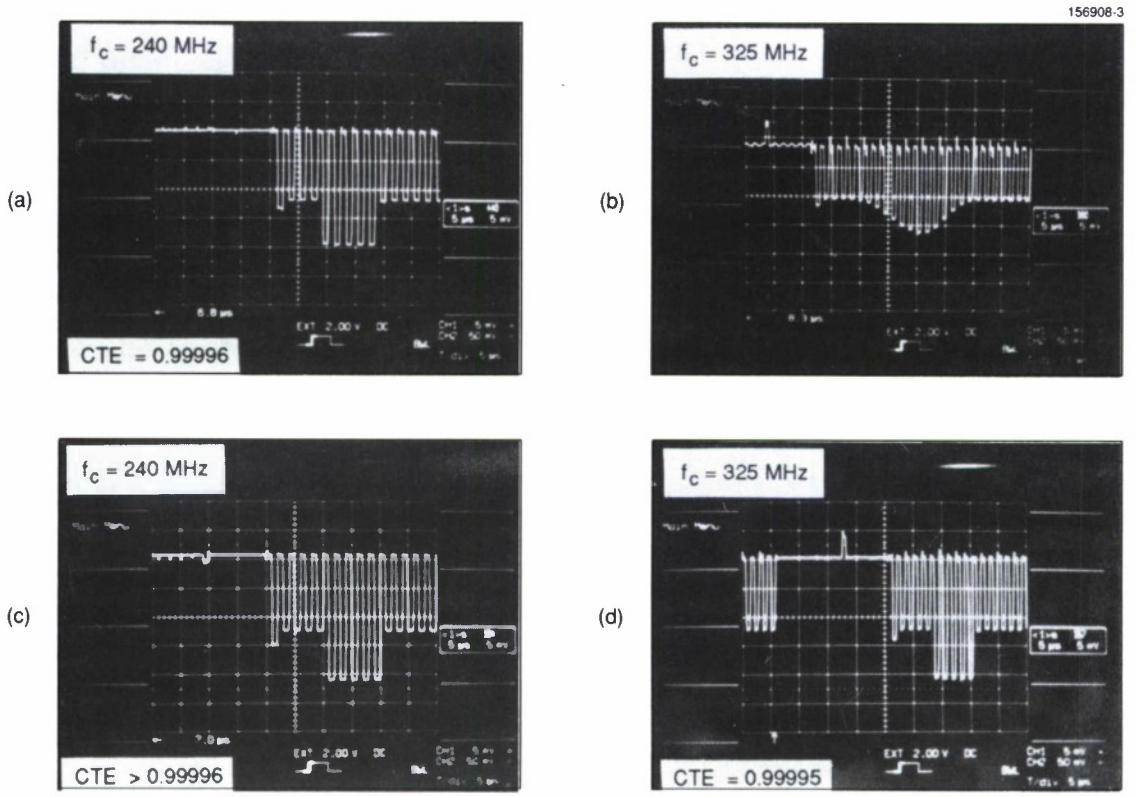

Figure 8. Output from the CCDs when the input is one pulse and five clock periods long for the following cases: (a) uniform doping, f_c = 240 MHz, (b) uniform doping, f_c = 325 MHz, (c) step doping, f_c = 240 MHz, and (d) step doping, f_c = 325 MHz.

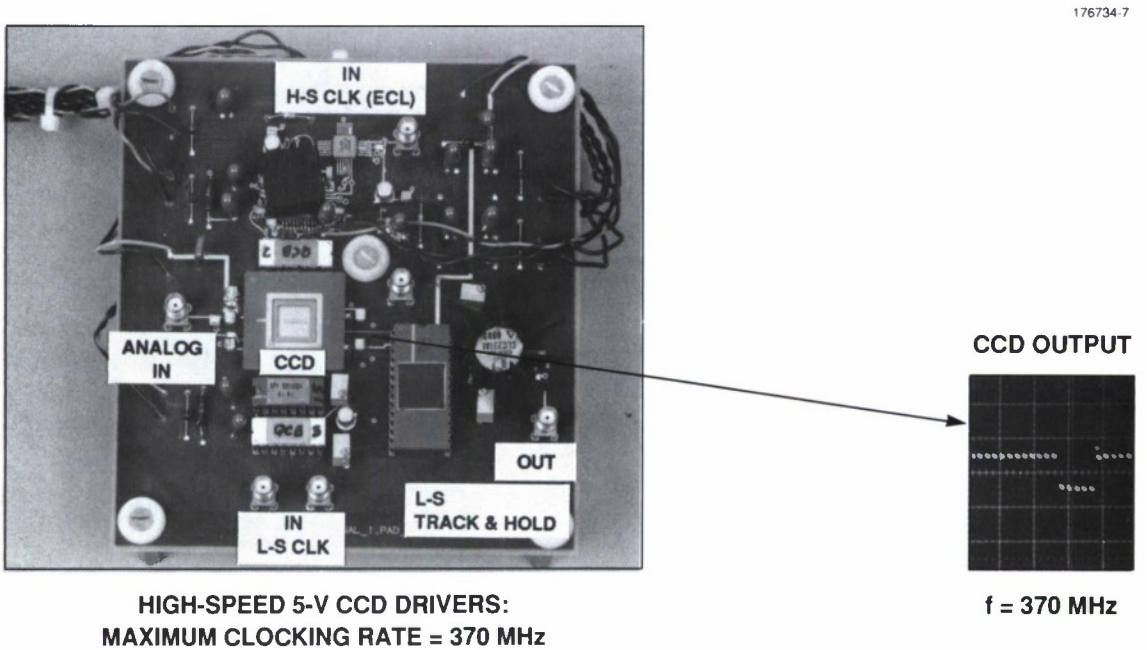

Figure 9. Multilayer board and output of the nonuniform, short-channel CCD for f_c = 370 MHz.

5. THE SPS MEMORY

An analog memory chip for high-speed data acquisition and slow readout (fast-in, slow-out mode) was also designed and included in the wafers. Although all-digital systems require many components, the CCD memory is compact and consumes very little power (< 50 mW). The chip has a serial-parallel-serial (SPS) architecture [6]. The memory consists of a high-speed input register (similar to the short-channel CCDs described in the previous sections), a parallel array, and a low-speed output register, and it can hold 128 × 128 (16 K) analog samples. A photograph of the chip is shown in Figure 10. The SPS memory operates as follows. During the fast-in time, the top register acquires 128 samples of the incoming signal. When the top register is full, its clocks are stopped, and the charge is transferred one stage down the parallel array at a rate that is 1/128th of the input rate. When the parallel array is full, after 128 parallel transfers, the charge is transferred line by line to the bottom serial register and read out at a slower rate, which is usually determined by the circuitry that follows the memory.

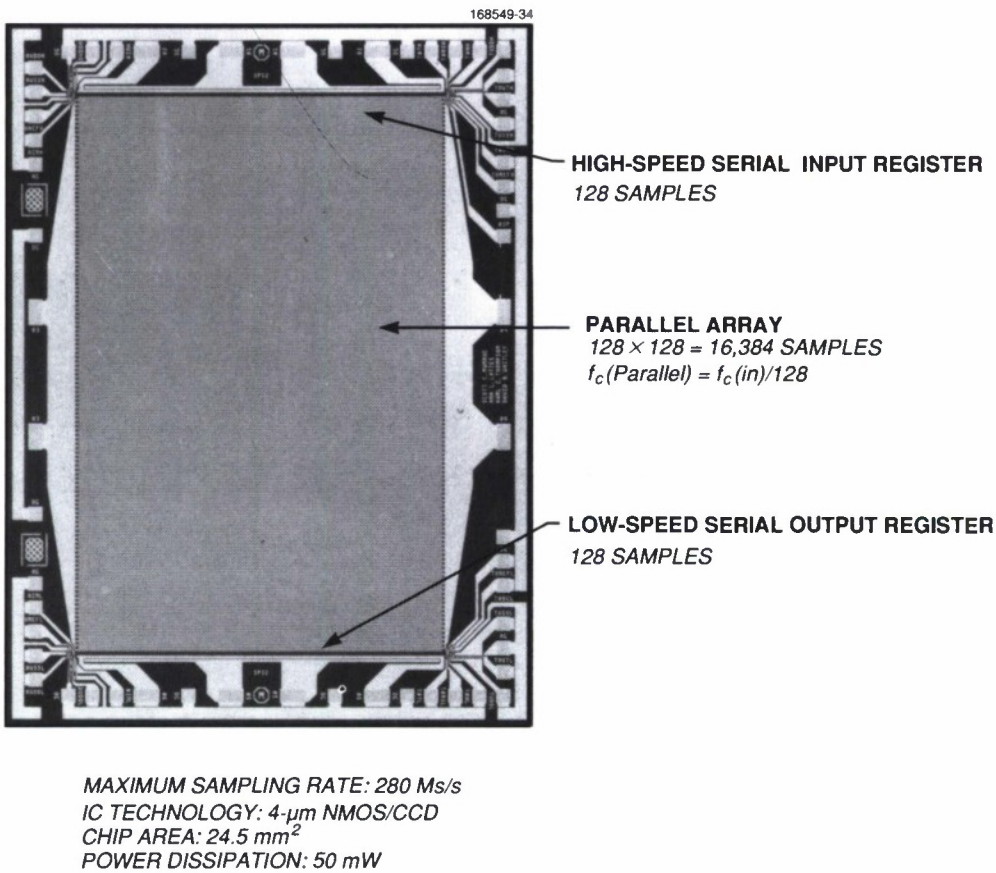

Figure 10. SPS CCD memory.

The input serial register consists of a two-phase CCD, 26 μm wide with 4-μm-long barrier gates and 7-μm-long storage gates. The storage wells have step doping to enhance the transfer speed. Because in the serial register of the SPS the charge transfer occurs in two dimensions, the step implant was tilted 4.4°. With this step-doping geometry, the enhancement of the drift fields is expected to occur mostly along the serial register where maximum speed is desired but also to some degree in the perpendicular direction where, because of the long gate length (26 mm), the fringing fields are very weak for the serial-to-parallel transfer. Figure 11 shows schematically the operation of the SPS. The oscilloscope traces show the high-speed input waveform (two negative-going pulses) and the low-speed output. The horizontal and vertical scales were adjusted so that the two traces could be lined up. The sampling rate was set at 280 MHz. The top of the input waveform was beyond the input range of the CCD so that the device was operated with no fat zero (worst-case condition). The bottom of the output pulses tracks very well to the bottom of the input pulses, while the top is flat because it is pinned at the zero-charge level. Beyond 280 MHz the CTE in the top register degrades very rapidly.

For comparison, SPS CCDs without the built-in fields were fabricated on the same wafers; the maximum clocking rate in the top registers of the uniformly doped CCDs was only 150 MHz. The serial-to-parallel transfer required at least 125 ns. This rate is generally consistent with the estimates from two-dimensional simulations and adequate for a serial-to-parallel transfer that is 1/128th of the serial rate. For the parallel transfer rate, there was no measurable difference between the uniform and step-doped CCDs. This result, while disappointing, is understandable because only a small fraction of the built-in fields are in the serial-to-parallel direction.

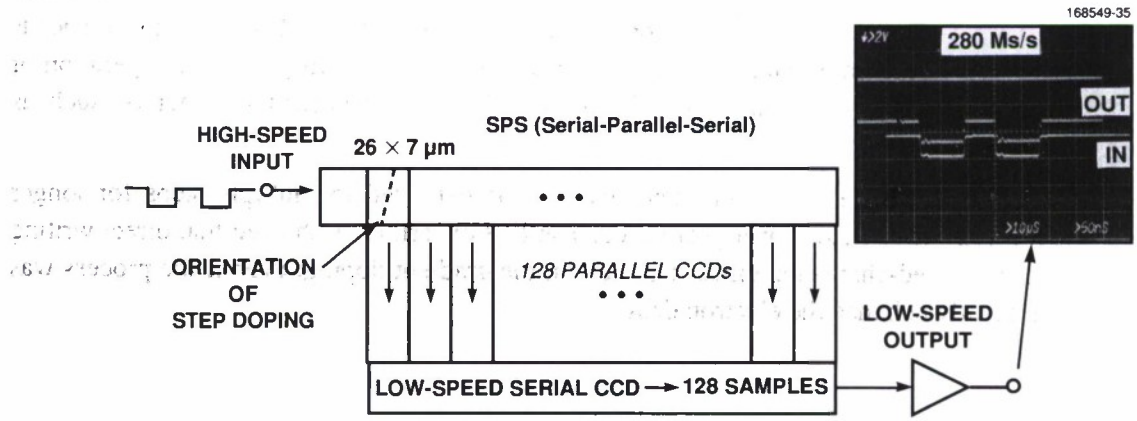

Figure 11. Schematic diagram illustrating the operation of the CCD analog buffer memory and the experimental results for a sampling rate of 280 MHz.

6. SUMMARY

A technique has been developed to improve the CTE in buried-channel CCDs while maintaining low clock voltages and large charge capacity. Given the limited resources of the IRP project, the development of a new process to optimize the CCD performance could not be accomplished. Nevertheless, in the current study, simulations were carried out to model the existing process, which was modified to incorporate built-in fields, and the performance of the CCDs was predicted using a simple steady-state model.

Testing the short-channel CCDs was the most challenging aspect of the project. Even with the custom-designed clock drivers, the maximum clocking rate of the step-doped CCDs could not be measured. Short-channel CCDs (L = 7 μm) with the built-in drift fields were tested up to 370 MHz (the limit of the existing clock drivers) with no measurable degradation in the charge transfer efficiency, although the equivalent uniform CCDs degrade at 240 MHz.

The performance of the long-channel CCDs (CTE at a given clocking rate) was dramatically improved with the built-in drift fields, even at low clocking rates, both at room temperature and at 77 K. Although these CCDs cannot achieve the record speeds observed with the short-channel CCDs, they are nevertheless extremely fast compared with uniform long-channel CCDs. The results are consistent with two-dimensional simulations that consider only the drift of a single electron traveling along a storage well.

A 16-K monolithic analog memory has been demonstrated that is capable of sampling incoming data at 280 MHz, storing it, and slowing it down so that it can be interfaced with conventional processors. Other CCD-based buffer memories have been demonstrated at hundreds of megahertz, but those speeds are achieved at the expense of memory size and require at least 10-V clocks. Only the basic operation of the device has been tested and its maximum speed determined. Other important parameters, such as linearity and dynamic range, remain to be determined.

The step implant is a simple processing step that can be extended to multiple steps for longer storage gates, a larger number of stages, or higher speed. The FIB experiments showed that direct writing is a viable technique for buried-channel engineering and that the gradient doping, even if the process was not optimized, could greatly enhance the electron drift.

7. CONCLUDING REMARKS

The built-in drift fields can provide the CCD designer additional degrees of freedom previously unavailable. For example, CCD gates or shift register lengths can be increased while preserving speed. Alternatively, the clock voltages can be reduced.

The results obtained and the simulation and testing expertise gained during this IRP project are directly applicable to current research work. A 5-V CMOS/CCD process [7] is being developed that requires low thresholds, high linearity, and uniphase 5-V clocking. The relative clock swing is half that of the two-phase CCDs, and the drift fields are correspondingly smaller. Shallow buried-channel profiles were engineered to maximize both the charge capacity and the speed. To maximize the drift fields, the barrier and storage levels are separated by 1.25 V. A CCD-based programmable analog-ternary correlator and a 64 K SPS memory are currently being designed with this process. The step doping will allow clocking of these CCDs at $f_{c(max)} > 200$ MHz.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	12 July 1991	Technical Report

4. TITLE AND SUBTITLE

Shallow-Buried-Channel CCDs with Built-In Drift Fields

5. FUNDING NUMBERS

C — F19628-90-C-0002

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TR-925

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

HQ Electronic Systems Division ESD/ENKL
Hanscom, AFB 01730-5000

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

ESD-TR-91-085

11. SUPPLEMENTARY NOTES

None

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (*Maximum 200 words*)

The performance of charge-coupled devices (CCDs) is limited by the charge that is left behind after the bulk of the charge packet has transferred by Coulomb repulsion. In the absence of drift fields these residual electrons will transfer by thermal diffusion, which is a very slow process. The CCD speed can be enhanced by designing structures with strong fringing fields between gates, such as deep-buried-channel CCDs. Deep-buried-channel delay lines have indeed been demonstrated at record speeds (hundreds of megahertz), but they have several disadvantages that may ultimately limit their usefulness. For example, the shape of the potential wells is distorted, degrading linearity and affecting the overall signal-processing performance of the CCD. Furthermore, the charge-handling capacity decreases as the channel moves into the bulk, and at least 10-V clocks are required. These 10-V clocks are not only difficult to generate at high speed, but are incompatible with the 5-V technology necessary for the high-performance on-chip support circuits that interface with the CCD.

To overcome these disadvantages a technique was developed to improve the charge-transfer efficiency (CTE) in buried-channel CCDs while maintaining low clock voltages and large charge capacity. Shallow-buried-channel delay lines with a channel depth of 300 nm were designed, fabricated, and tested. These delay lines operate with 5-V two-phase clocks and have a built-in potential gradient to improve the CTE. Long-channel CCDs with storage gates 26 μm long and short-channel CCDs with storage gates 7 μm long were studied. In both cases the barrier electrodes are 4 μm long. The built-in fields were generated by a longitudinally nonuniform implant in the storage wells.

Two types of short-channel CCDs were tested: uniform and step-doped CCDs. The nonuniform CCDs were tested up to 370 MHz. Three types of long-channel CCDs were tested: uniform, step-doped, and gradient-doped CCDs.

The results are consistent with CCD modeling performed with CANDE, a two-dimensional device simulator.

14. SUBJECT TERMS

charge-coupled devices (CCDs) high speed
buried-channel

15. NUMBER OF PAGES
34

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	SAR